In the Specification

Please replace the paragraph beginning at page 6, line 13 with the following paragraph:

FIG. 6 shows an example of how the scrambled output value is generated for output bit Dout(50) identified as item 66. The scrambled value for Dout(50) is derived using the relationship NS(7)^NS(27)^NS(46)^Din(11)^Din(50). Bits 66 represent the scrambled output bits for a current clock period, and bits 68 represent the scrambled output bits for a previous clock period. The 39th polynomial X(39) for Dout(50) is the scrambled output bit Dout(11) identified as item 70 in FIG. 6. The scrambled value Dout(11) is derived from the equation NS(27)^NS(46)^Din(11) (FIG. 4). The 58th polynomial X(58) for Dout(50) is Dout(56) and is identified as item 71 from bits 68. The value of Dout(56) is loaded into new seed register NS(7).

Please replace the paragraph beginning at page 6, line 25 with the following paragraph:

Referring to FIG. 7, a N-bit parallel data de-scrambler 79 is similar to the scrambler shown in FIG. 2. The de-scrambler 79 includes an input data register 82, scrambling logic 90, new seed register 86, and an output data register 94. The scrambled parallel input data stream 80 is loaded into the input data register 82 at the rising edge of a current clock period generated by the clock circuit 96. During a next clock period, the de-scrambling circuit 90 de-scrambles every bit of the scrambled parallel data stream 80 with the de-scrambling polynomial 1+X(39)+X(58) using the parallel input data from data register 82 and the preloaded new seed values 88 pre-loaded into the new seed register 86 during a previous clock period.